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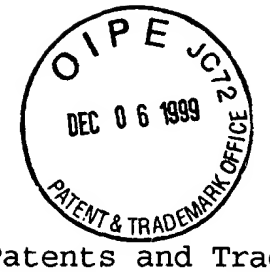
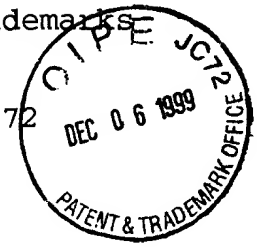
Linda B.



November 29, 1999

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231



Fr: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
Poughkeepsie, N.Y. 12603

Subject: Serial No. 09/418,031 10/14/99

S.M. Jang, C.S. Liu, C.H. Yu

DAMASCENE METHOD EMPLOYING
COMPOSITE ETCH STOP LAYER

Grp. Art Unit: 1765

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 5,380,679 to Kano, "Process for Forming a Multilayer Wiring Conductor Structure in Semiconductor Device", discloses a method for forming a multi-level conductor wiring structure in a microelectronics fabrication affording improved adhesion between layers with no additional photolithographic steps.

U.S. Patent 5,451,543 to Woo et al., "Straight Sidewall Profile Contact Opening to Underlying Interconnect and Method for Making the Same", discloses a method for forming vertical sidewalls when etching via contact holes through intermediate dielectric layers over conductor lines and lands.

U.S. Patent 5,818,110 to Cronin, "Integrated Circuit Chip Wiring Structure with Crossover Capability and Method of Manufacturing the Same", discloses a method for forming multi-layer dual damascene interconnection layers without requiring interlock vias.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37661